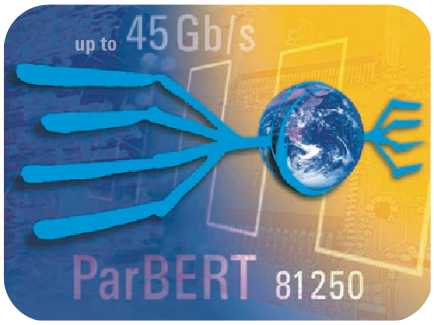
Agilent ParBERT 81250 40 Gbit/s Parallel Bit Error Ratio Test Solutions

Product Overview
Version 1.9

Accelerate Your Time to Market with the Ideal Electrical/Optical Solutions for Testing Both the Parallel and Serial Sides of OC-768 for the 40G Wave



Agilent Technologies

Agilent 40 Gbit/s ParBERT Solutions for Electrical/Optical OC-768 Applications

The Agilent family of 40 Gbit/s ParBERT products, ParBERT 43.2G and 45G, is the ideal solution for bit error ratio (BER) testing of both, the parallel and serial sides of optical and electrical OC-768. They enable fast time-to-market by testing all critical optical/electrical elements in OC-768 digital transmission lines - from components and modules up to line cards.

The 40G solutions are based on the modular and flexible ParBERT platform. Since its introduction in the year 2000, ParBERT triggered a paradigm shift in the BER market. It gained the Test and Measurement World "2003 Best in Test" award recently.

The ParBERT 81250 40G family is optimized to address the following applications:

- **Serial Test**
Test transimpedance amplifiers (TIAs), clock recovery circuits, laser drivers etc., up to 45 Gbit/s (depending on the configuration).

- **OC-768 16:1 MUX/DeMUX Test**
Directly stimulate and analyze 1:16 multiplexers (MUXes) and demultiplexers (DeMUXes) up to 45 Gbit/s as well as the 2.7 Gbit/s or 3.35 Gbit/s tributary data rates.

- **SFI-5**
The unique ParBERT modularity easily allows the stimulation and analysis of additional channels according to the SFI-5 (SerDes-Framer Interface Level 5) standard, e.g. the deskew channel.

- **OC-768 4:1 MUX/DeMUX Test**
Additional channels at 10.8Gbit/s are available for OC-768 4:1 MUX/DeMUX testing.

- **FEC device test**
Test at 43.01841 Gbit/s, the Forward Error Correction (FEC) data rate resulting from the 255/236 overhead.

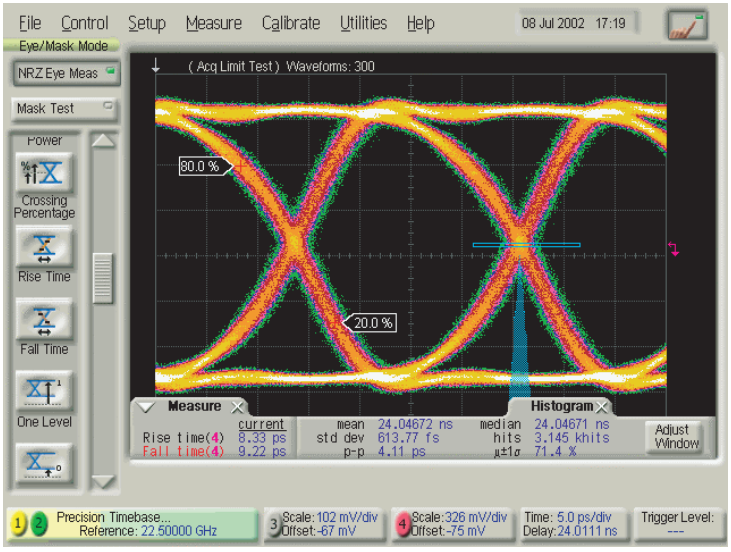
- **OC-768 Optical System**
The ParBERT 40G Electrical/Optical System solutions enable testing BER for all serial line optical and electrical applications. Data formats available are NRZ, RZ and RZ-CS for the C and L bands.

- **Recirculating Loop**
Control a recirculating loop setup with ParBERT's unique Sequence Editor. This allows e.g. a time aligned control of acoustic optical modulators to switch burst data through the loop. With its "Fast Synchronization Mode" feature, ParBERT 81250 40G is able to lock and synchronize onto a burst data stream.

Table of Contents

1.0 ParBERT 81250 40G Key Features Overview

- excellent waveform with good jitter performance and low overshoot and ringing, see Fig. 1
- depending on the configuration, Pattern Generator and Error Detector run up to 45 Gbit/s on the serial side and up to 10.8 Gbit/s on the parallel side within one system; ideal for testing the parallel and serial sides of OC-768 16:1 and 4:1
- Error Detector with built-in CDR (Clock Data Recovery); this is key for most applications in which the clock versus data changes/drifts Unique
- variable output levels up to 2 Vpp
- variable threshold and sampling delay with the DeMUX E4869B New
- modularity allows to build individual test configurations which will adapt to most application requirements; multiple modules of any speed class can be added to the system
- optical interface available as an upgrade; ParBERT 45G Optical offers NRZ, RZ and RZ-CS Unique
- the flexible and expandable platform provides investment protection as modules can be added over time
- data rate subranges at 2.5 Gbit/s, 10 Gbit/s and 20 Gbit/s, with 40 Gbit/s transition times and jitter! Unique New
- fast synchronization on burst data, allows to run recirculating loop tests
- choice of data sequences: user-defined, memory-based patterns, PRBS patterns up to 2^{31}-1, Errored PRBS pattern, Variable Mark Density PRBS patterns
- quick generation of data sequences with PRBS, memory-based patterns and pause 0/1 blocks with multiple levels to loop indivual data blocks with the Sequence Editor
- SONET/SDH Frame Generator and SFI-5 test software tool
- remote access via LAN or GPIB
- programming with Agilent VEE, National Instruments Labview®, Agilent TestExec, C/C++, Microsoft® Visual Basic and Excel; programming requires no hardware!



- output of the Pattern Generator E4896A (MUX E4868B), measured with 86118A DCA remote head, 86107A precision time base and 12" cable
- frequency: 45 Gbit/s
- amplitude: 2 Vpp
- jitter: 613 fs in this waveform (700 fs rms typical)
- rise time 8.3 ps and fall time 9.2 ps in this waveform (9 ps typical)

Figure1: ParBERT 45G waveform example

1.1 Data Rate Subranges at 5 Gbits/s, 10 Gbit/s and 20 Gbit/s

The ParBERT 40G family provides data rate subranges at 5 Gbit/s, 10 Gbit/s and 20 Gbit/s. The fast transition time and the leading jitter performance of the 40G waveform (9 ps typ. and 700 fs rms typ.) are maintained. All PRBS polynomials up to 2^{31}-1 are supported.

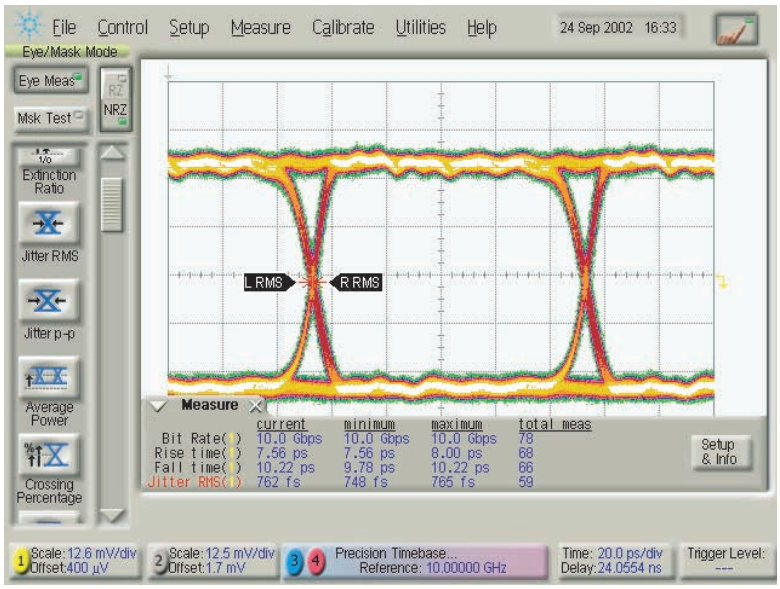
For ParBERT 45G, the available data rates are:

- 38 Gbit/s - 45 Gbit/s
- 19 Gbit/s - 22.5 Gbit/s
- 9.5 Gbit/s - 11.25 Gbit/s
- 4.74 Gbit/s - 5.625 Gbit/s
- 2.37 Gbit/s - 2.81 Gbit/s

An example is given in Figure 2.

For ParBERT 43.2G, the available data rates are:

- 38 Gbit/s - 43.2 Gbit/s
- 19 Gbit/s - 21.6 Gbit/s
- 9.5 Gbit/s - 10.8 Gbit/s
- 4.74 Gbit/s - 5.4 Gbit/s
- 2.37 Gbit/s - 2.7Gbit/s



- **risetime: 7.56ps**
- **falltime: 10.22ps**
- **jitter: 762fs rms**

Figure 2: PaRBERT 45G 10 Gbit/s data rate subrange, waveform for PRBS 2^{31}-1, 0.5 Vpp amplitude

1.2 ParBERT Ease-of-use

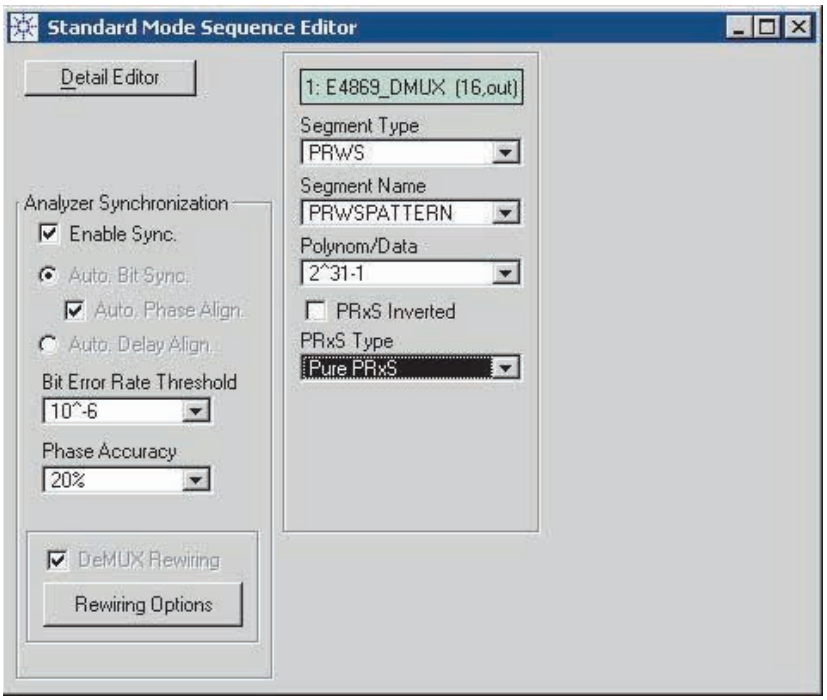


Figure 3: Sequence editor showing how to setup PRxS, memory-based patterns

The ParBERT 81250 45G Graphical User Interface (GUI) has a powerful Sequence Editor (Fig. 3) and includes the control of the Pattern Generator MUX module and the Error Detector DeMUX module (see Figs. 4 & 5).

Pattern Generator and Error Detector are set up in four steps:

- select a user-defined or a predefined frequency.
- set up the variable amplitude (up to 2 Vpp) and the threshold a (range ±400 mV).
- select the clock system (internal or external clock).
- select the data pattern, e.g PRxS polynomial 2^{31}-1 or user-defined memory-based patterns.

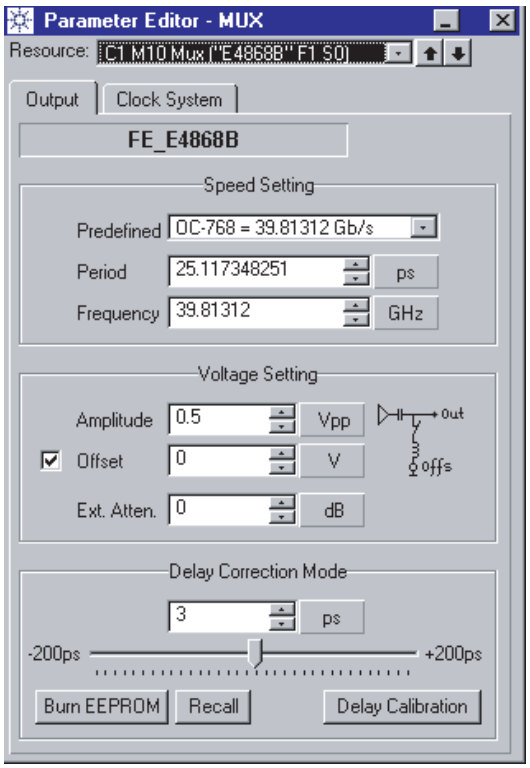


Figure 4: MUX property window

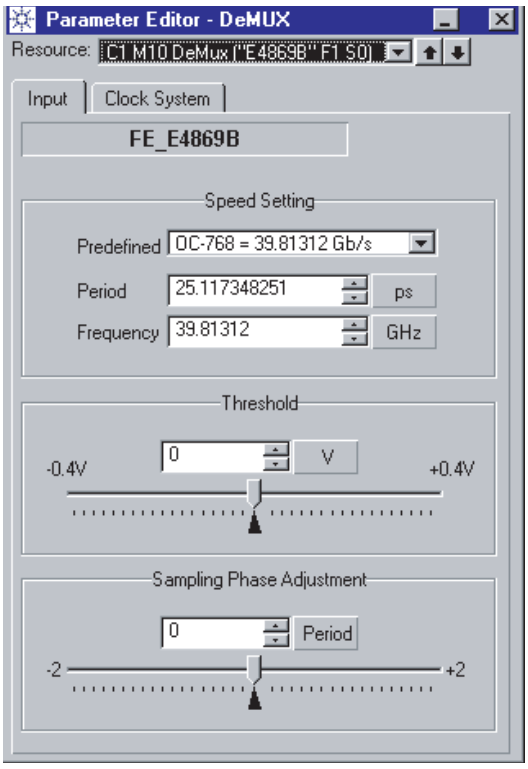


Figure 5: DeMUX property window

1.3 ParBERT 81250 enhanced Bit Error Ratio Measurement

The bit error ratio (BER) measurement allows you to determine the ratio of error bits versus the total number of bits received from a device under test (DUT) with one or several output ports and associated terminals.

The Agilent 81250 GUI already includes a simple bit error rate measurement. The Measurement Software provides enhanced capabilities.

Bit Error Ratio Measurement Modes

The bit error ratio measurement of the ParBERT Measurement Software (example see Fig. 6) can be run in two modes:

- The Single Mode is similar to the standard BER test of the GUI. However, this mode is also able to differentiate between errors on 1s(logical 1 expected, but logical 0 received) and errors on 0s (logical 0 expected, but logical 1 received). Even more important, it is possible to specify one or several stop criteria. This can be used todefine conditions which allow the user to compare the measurement results of several executions or devices at a glance.

- The Repetitive Mode is mainly used to measure the long term stability of a device. In this mode, the measurement is divided into time intervals of equal duration. The results can be saved in a log file. This file contains one record for each measurement interval. The log file, which can be imported into any spreadsheet or text processing program, allows investigation of any changes in the bit error ratio due to time, temperature, humidity, or other varying conditions. This helps to obtain reli-

Measurements provided:

- BER (ALL) - the number of bits in error divided by the number of received bits
- Compared Bits - the total number of compared bits
- # of errors - total of all bits in error
- 0 BER - counts the number of bits where logical zero was expected but logical one received
- 1 BER - counts the number of bits where logical one was expected but logical zero received
- # of 0 Errors - the number of errors where logical zero was expected but logical one received
- # of 1 Errors - the number of errors where logical one was expected but logical zero received

Bit Error Rate4-Running

Start: 12/02/02 08:22:13 Single Mode

Port/Terminal	Reset	Actual BER	Actual Compared Bits	Accumulative Compared Bits	Accumulative BER	Actual 0 BER	Actual 1 BER
Measurement							
[1] E4869_DMUX		0	4e+010	6.81e+011	0	0	0
[1:1] T1		0	2.5e+009	4.26e+010	0	0	0
[1:2] T2		0	2.5e+009	4.26e+010	0	0	0
[1:3] T3		0	2.5e+009	4.26e+010	0	0	0
[1:4] T4		0	2.5e+009	4.26e+010	0	0	0
[1:5] T5		0	2.5e+009	4.26e+010	0	0	0
[1:6] T6		0	2.5e+009	4.26e+010	0	0	0
[1:7] T7		0	2.5e+009	4.26e+010	0	0	0
[1:8] T8		0	2.5e+009	4.26e+010	0	0	0
[1:9] T9		0	2.5e+009	4.26e+010	0	0	0
[1:10] T10		0	2.5e+009	4.26e+010	0	0	0
[1:11] T11		0	2.5e+009	4.26e+010	0	0	0
[1:12] T12		0	2.5e+009	4.26e+010	0	0	0
[1:13] T13		0	2.5e+009	4.25e+010	0	0	0
[1:14] T14		0	2.5e+009	4.25e+010	0	0	0
[1:15] T15		0	2.5e+009	4.25e+010	0	0	0
[1:16] T16		0	2.5e+009	4.25e+010	0	0	0

Figure 6: Bit Error Ratio windows

1.4 SONET/SDH Frame Generator

The SONET/SDH Frame Generator is a software application for generating SONET and SDH frames for the ParBERT 81250.

The Frame Generator allows structured patterns (also known as frames) to set up and generate for SONET/SDH testing with the 81250. It provides a Graphical User Interface for entering basic frame patterns, and allows the manual modification of the resulting frame files.

81250 SONET/SDH Frame Generator are depicted in figure 7:

- Mode:
  - Normal specifies a single frame of a SONET/SDH signal
  - CID specifies a Consecutive Identical Digit pattern
- Format:
  Defines the frame format; can either be SONET, SONET-C, or SDH
- Scrambler:
  Selects the scrambling of the payload; the SONET/SDH 2^7-1 PRBS standard is used for the scrambling
- CMI:
  Selects the Coded Mark Inversion format, which doubles the data rate
- Payload
  - All zeros
  - All ones
  - Alternate 1, 0
  - Various PRBS settings
  - Edit pattern
  - From file
- Errors
  - L-BIP (B2)
  - S-BIP (B2)
  - P-BIP (B3)
  - None
- Alarms
  - OOF
  - L-AIS
  - L-FERF
  - P-FEBE
  - None
- Mask Analyzer B Bytes

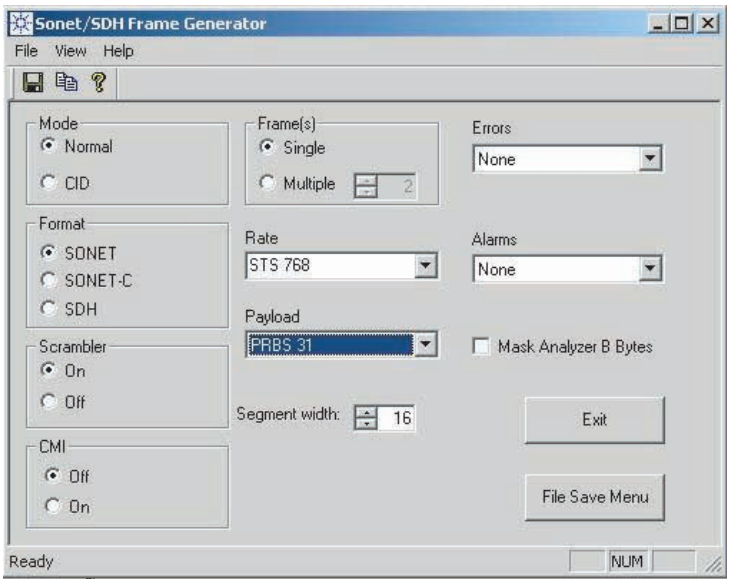


Figure 7: SONET/SDH Frame Generator

The parameters of the ParBERT

2.0 ParBERT 40G System Architecture

ParBERT 81250 hardware is based on the recognized industry-standard VXI.

All 40G ParBERT 81250 systems with three VXI mainframes (example see Fig. 8) are integrated in a rack.

An optional rack PC, flat panel monitor with mouse and keyboard and supporting arm are available.

The main components and the data flow of an 81250 45G Electrical/Optical system are give in Fig. 9:
- 45 Gbit/s Pattern Generator E4896A (1)
- 45 Gbit/s Error Detector E4897A (2)
- 45 Gbit/s Lightwave Transmitter (E/O converter) E4883A (3)
- 45 Gbit/s Lightwave receiver (O/E converter) E4882A (4)

In conjunction with a ParBERT 81250 40G system an 86100 DCA (Digital Communications Analyzer) should be used with the appropriate bandwidth.

Figure 8: ParBERT 45G Electrical/ Optical front-view

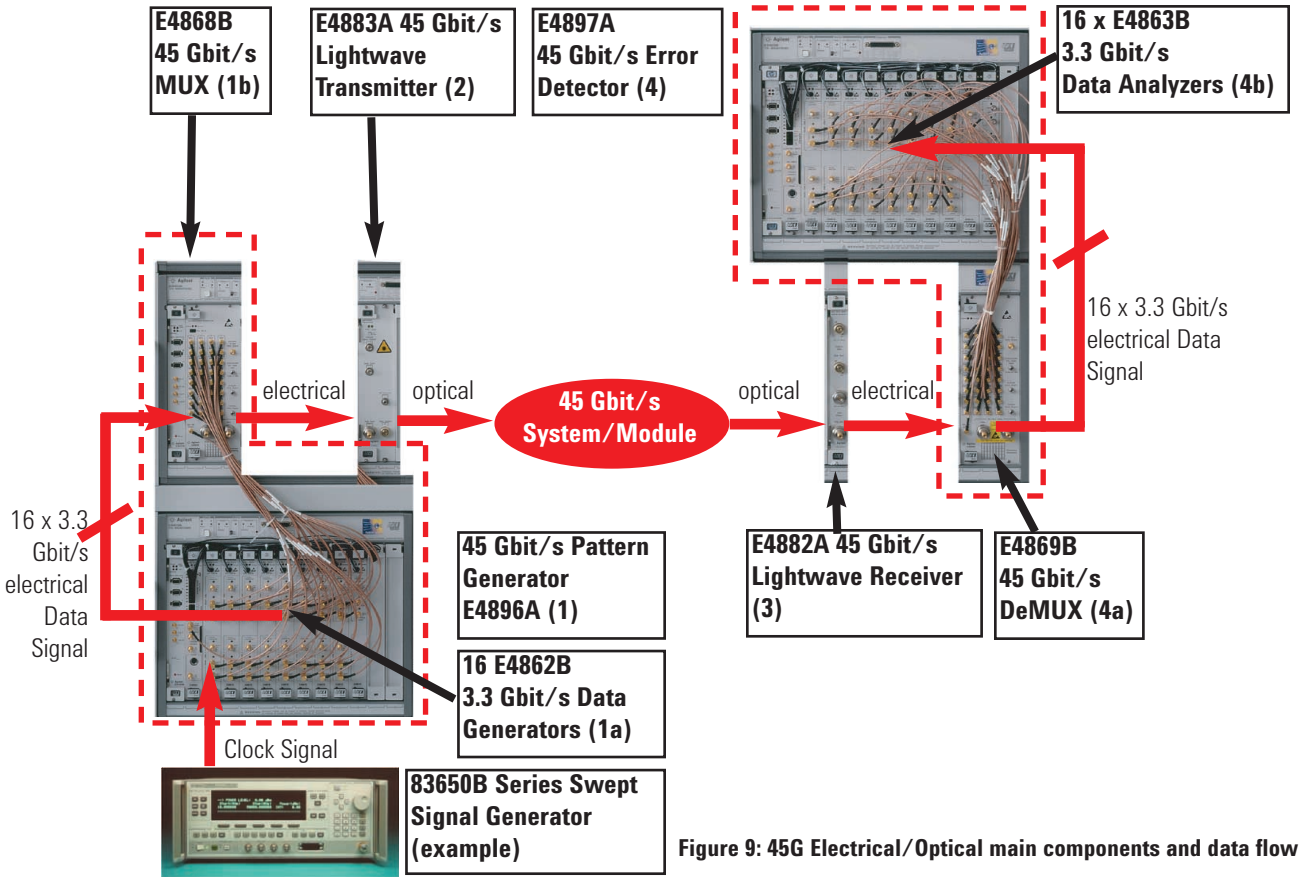


Figure 9: 45G Electrical/Optical main components and data flow

For the details and data flow of a ParBERT 45G electrical/optical system, refer to Figure 9. The Pattern Generator E4896A is a combination of the 16 tributary 3.35 Gbit/s data generators (E4862B) and one MUX module (E4868B) . The Error Detector E4897A is a combination of a DeMUX module (E4869B) and 16 tributary 3.35 Gbit/s data analyzers (E4863B).

- the 16 data generators (1a) provide a parallel electrical data stream to the MUX (1b) which trans lates it to a serial 40G data stream
- the electrical output of the MUX is converted to an optical signal by the Lightwave Transmitter (2)
- the optical output of the DUT is fed to the Lightwave Receiver (3) which converts it to an electrical 40G serial data stream
- the DeMUX (4a) distributes the data stream to the 16 data analyzers (4b) which make the BER measurement

E4868B MUX Module

with subrate clock input/output

The MUX module is a 16:1 multiplexer. The 16 differential data inputs on the parallel side are connected with 32 cables to 16 data generator channels (2.5 Gbit/s or 3.35 Gbit/s). The MUX module also includes a clock distributor which provides sub-rate clocks at 1/2, 1/4 and 1/16 or 1/64 of the master period. The internal oscillator can be substituted with an external source connected to the external clock input, e.g. a signal generator, with subrates still available.

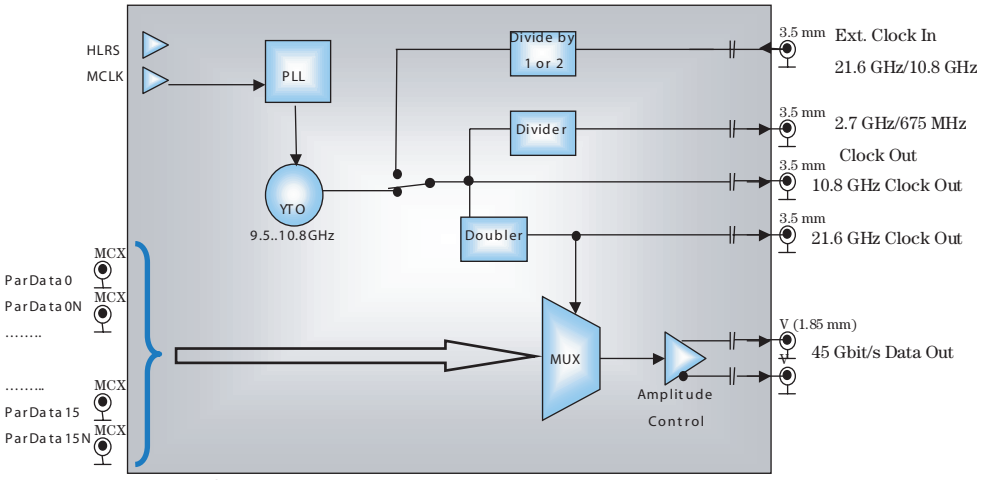


Figure 10: MUX module architecture

E4869B DeMUX Module

with built-in CDR

The DeMUX module can operate in two modes:

- CDR (Clock Data Recovery) mode
- external clock mode

In the CDR mode the module recovers the clock from the data input. It is not necessary to supply a clock to the module in this mode.

In the external clock mode the clock phase in reference to the data phase has to be controlled externally with a phase-shifter.

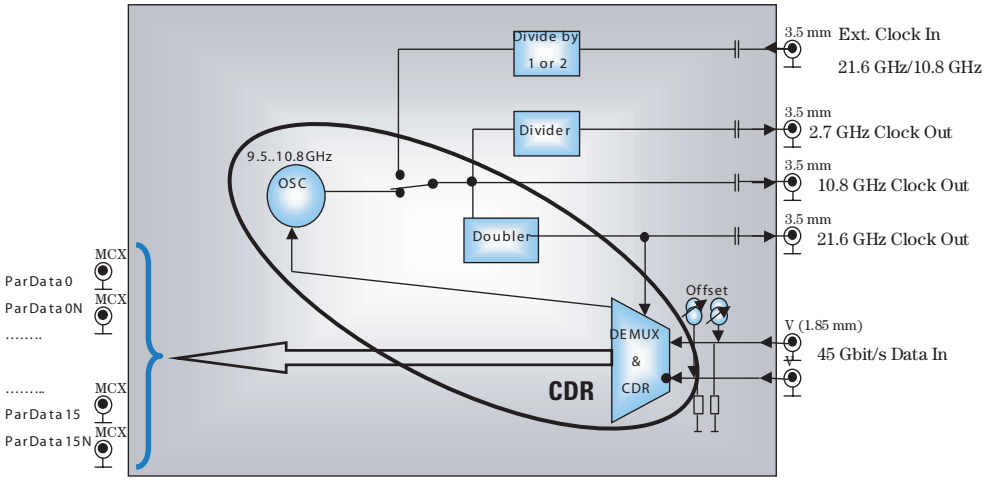


Figure 11: DeMUX module architecture

3.0 ParBERT 40G Use Models

Six key applications are:

3.1 40G serial BER testing (electrical)

The family of Agilent ParBERT 40G Pattern Generators and Error Detectors is ideally suited for serial BERT testing.

The 40G Pattern Generator provides a differential output of PRBS or memory-based pattern in NRZ format. Additionally, clock subrate outputs are available as well.

In the example shown in figure 12 (E8274C). The internal oscillator of the clock module (E4808A) is used as clock for the mux module and the tributary data generators.

The 40G error detector takes the NRZ data stream and provides CDR (clock data recovery). The recovered clock is used to keep the data processing of either PRBS or memory-based data in the proper clock phase.

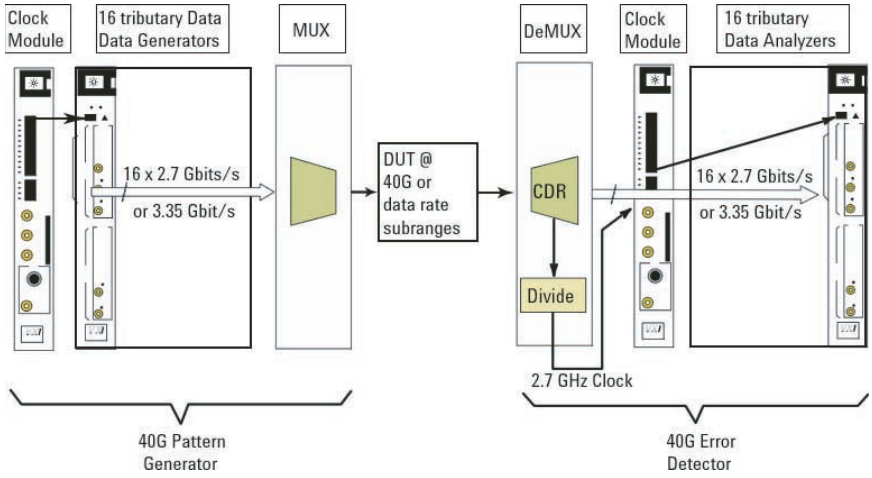


Figure 12: 40G Serial BER testing

For the new data rate subranges, please refer to paragraph 1.1.

3.2 OC-768 MUX Test

In order to set up a MUX test, the clock system of the MUX needs to be selected first.

Several alternatives are available for an internal or external clock source, as shown in Figs. 13 and 14.

The two most common alternatives for the clock set up are:

1. External Clock: This is the most flexible setup (Fig. 13) external signal generator, eg E8274C, which provides a master clock with improved phase noise characteristics.

The tributary generators of a 40G Pattern Generator can be used. Proper cabling then nees to be connected by the user (refer to Chapter 5.1 for details)

2. Internal Clock: The most economical setup (Fig. 14) It just provides a 675 MHz or 2.7GHz clock signal by means of a 17th generator channel. The analyzer consists of a full 40G Error Detector.

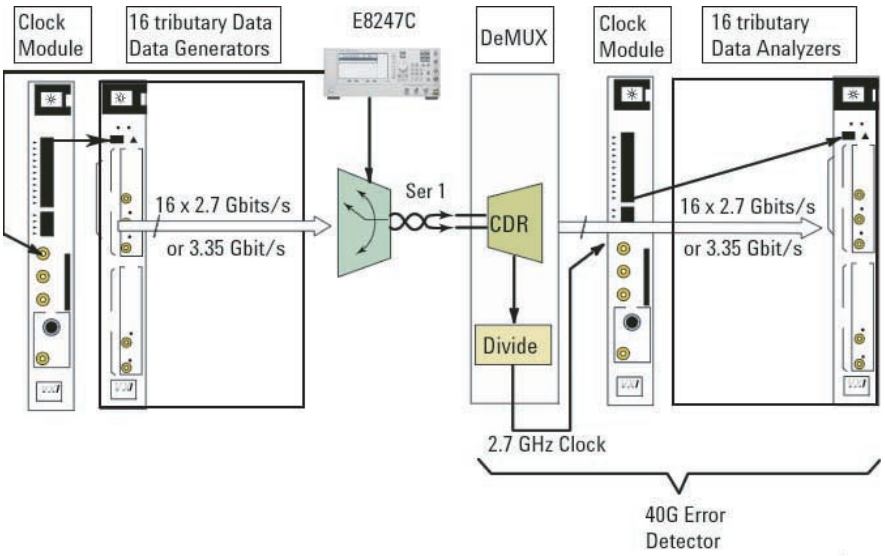


Figure 13: MUX test setup with internal MUX

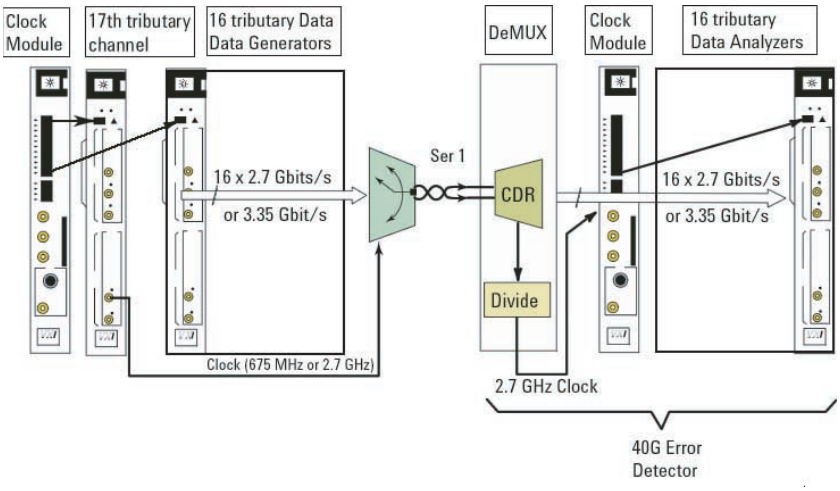


Figure 14: MUX test setup without internal MUX

3.3 OC-768 DeMUX Test

In the DeMUX test setup a 40G Pattern Generator is used to stimulate the DeMUX.

For the analysis, 16 analyzers at 2.7 Gbit/s or 3.35 Gbit/s are needed. They require the E4808A 10G clock module, which receives the recovered clock for reference (see Fig. 15). The tributary analyzers of a 40G Error Detector can be used. Proper cabling then needs to be connected by the user (see 5.2 for further details).

Some consideration should be given to the kind of measurement that is desired. The setup in figure 15 is for pure BER testing. For further testing on the DeMUX output timing (clock vs. data, see chapter 1.3), it is recommended that a 17th analyzer channel is connected to the recovered clock (see figure 16).

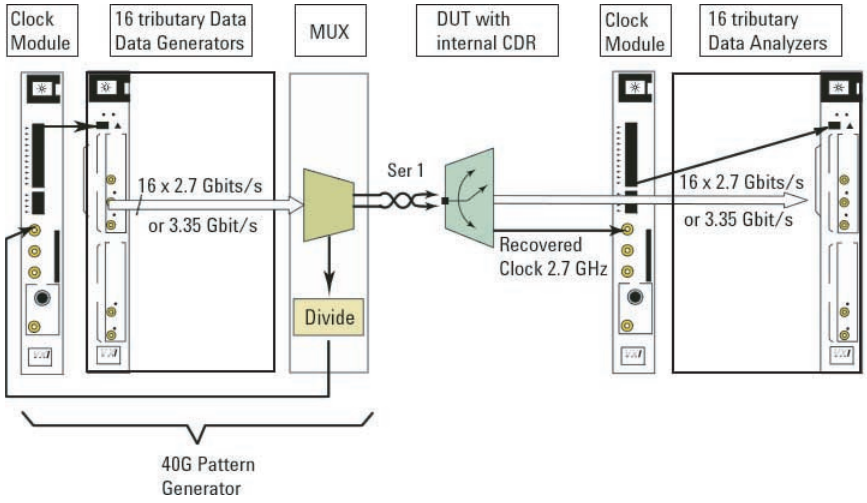


Figure 15: DeMUX test setup with 16 Analyzers

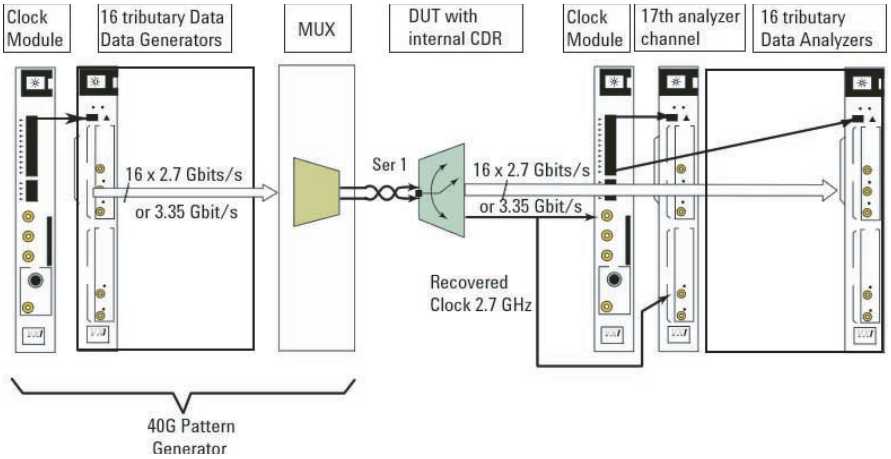


Figure 16: DeMUX test setup with 17 analyzers

3.4 SFI-5 Test Setup

The SFI-5 (Serializer/ Deserializer Framer Interface Level 5) standard addresses interfaces for packet and cell transfer in applications requiring 40 Gbit/s speeds. It promotes interoperability between complementary framer and forward-error-correction devices.

The key benefit of the SFI-5 standard is that it eliminates the need for a laborious and time-consuming deskew of the parallel tributary generator and analyzer channels. This is achieved by means of an addtional, 17th channel, that carries the information needed for the deskew integrated in the MUX. In the example given in figure 17, the 17th channel is denoted as TXDSC. By adding one more channel, ParBERT can even be used to generate the clock signal for the CDR of the SFI-5 MUX (TXDCK)

SFI-5 specifies a 16:1/1:16 multiplexing/demultiplexing architecture capable of handling data rates from 2.488 Gbit/s to 3.125 Gbit/s. ParBERT can generate SFI-5 formatted data and also receive and analyze it.

The Agilent 81250 ParBERT User Software supports SFI-5 device tests by providing two dedicated tools and a special data segment:

- The SFI-5 Frame Generator generates data that is for matted according to the SFI-5 standard.
- The SFI-5 Post Processing Tool analyzes captured SFI-5 patterns to determine the channel skew and BER.
- The SFI-5 data segment allows the generation of SFI-5 formatted data directly in the ParBERT hardware, pro vided that E4861B data gen erators and analyzers are used.

The unique ParBERT flexibility and scalability allows the user to define and specify the number of channels required for data rates specific to the SFI-5 set ups.

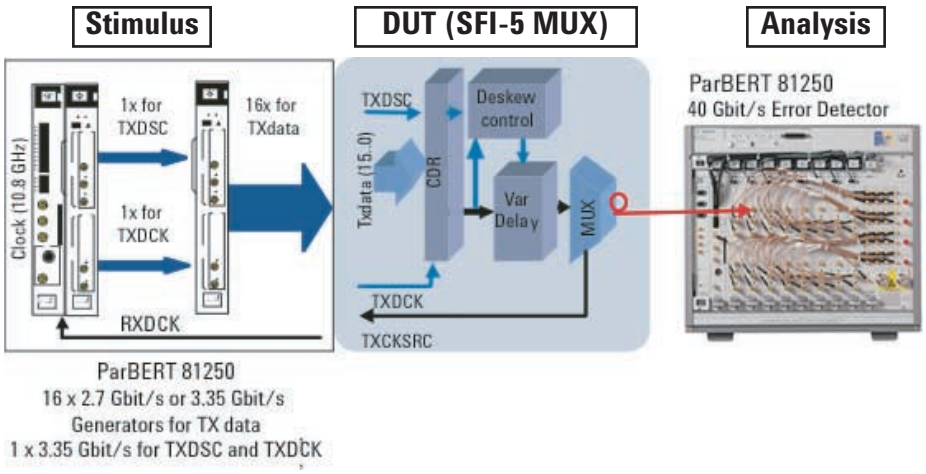


Figure 17: SFI-5 DeMUX Test Setup

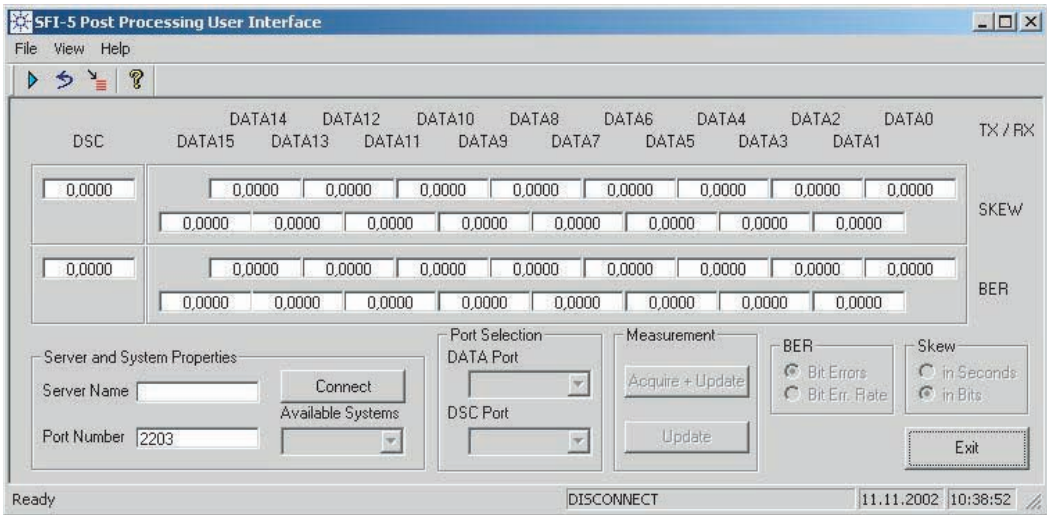


Figure 18: SFI-5 Post Processing Tool

3.5 Recirculating Loop Test

The recirculating loop setup allows the emulation of very long fibre systems with only a few fibre spans in an R&D labratory. Longhaul data transmission can then be tested with burst data. The Error Detector must be able to detect and synchronize on the burst data stream and read the data. The loop setup is controlled via a PC which controls the accoustic-optical modulator (AOM) switches to fill and open the loop (Fig. 19).

ParBERT 40G with its built-in CDR (Clock Data Recovery) is able to detect and synchronize on burst data and read BER measurements. The CDR is necessary to handle the phase shift of the bursted data stream.

The flexible ParBERT architecture is even able to control the AOMs using additional generator channels controlled via the Graphical User Interface. The entire loop can be controlled by the ParBERT PC controller and software. The ParBERT Sequence Editor (see Fig. 20) allows a time-aligned data processing to control the loops as well as to synchronize on the burst data. ParBERT 40G provides the ability to test the recirculating loop setup at 40 Gbit/s data rates but also at the subranges of 2.5 Gbit/s,
5 Gbit/s, 10 Gbit/s and
20 Gbit/s.

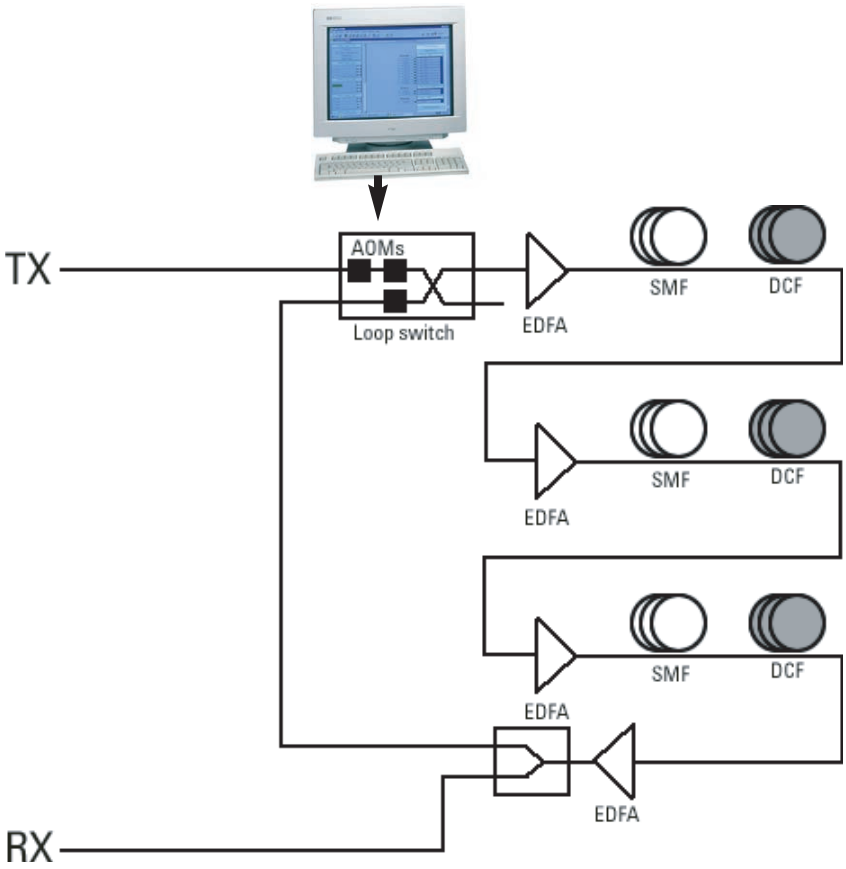


Figure 19: Recirculating Loop Setup

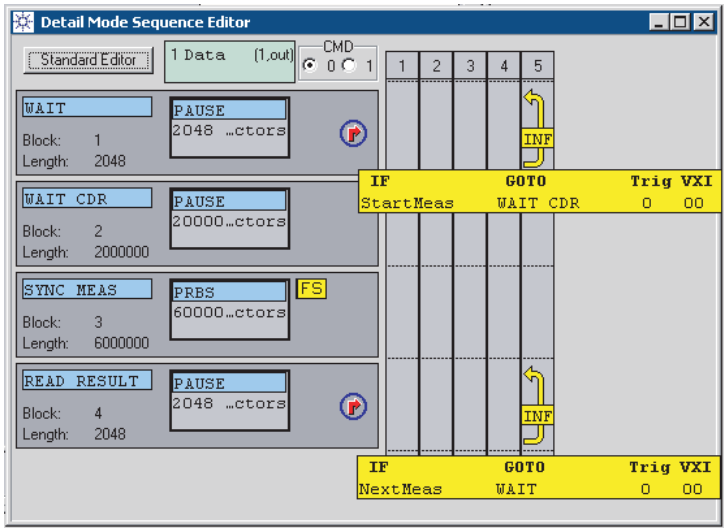


Figure 20: Control of AOMs for Recirculating Loop measurements

Unique

3.6 Electrical/Optical 40G Measurements

By adding 40G interface modules (Lightwave Transmitter and Lightwave Receiver), the ParBERT 81250 can be used to measure either electrical or optical inputs or outputs. The High Performance Option for the Optical Transmitter allows testing of the sensitivity of the DUT, and creation of sensitivity plots with BER versus optical attenuation.

With ParBERT 40G Electrical/Optical, the following devices can be tested:
- MUX/DeMUX devices
- electrical-to-optical devices
- optical-to-electrical devices
- optical-only devices
- electrical-only devices
- OR any combination of the above.

The Optical Transmitter data formates available are NRZ, RZ and RZ-CS for the C and L bands.

Figure 21: ParBERT 40G Electrical/Optical

4.0 Specifications of the Electrical System

4.1 System Specifications

The system specifications depend on the configurations and are given in Table 1.

Table 1: System Configurations & Specifications

Configuration	Pattern Generator E4894B, Error Detector E4895B	Pattern Generator E4896A, Error Detector E4897A
Data rate range	38 Gbit/s - 43.2 Gbit/s	38 Gbit/s - 45 Gbit/s
Data rate subranges	19 Gbit/s - 43.2 Gbit/s	19 Gbit/s - 45 Gbit/s
	9.5 Gbit/s - 10.8 Gbit/s	9.5 Gbit/s - 11.25 Gbit/s
	4.74 Gbit/s - 5.4 Gbit/s	4.74 Gbit/s - 5.625 Gbit/s
	2.37 Gbit/s - 2.7 Gbit/s	2.37 Gbit/s - 2.81 Gbit/s
Memory	128 (16 x 8) MBit	256 (16 x 16) MBit
pure PRBS	2^n-1, n = 5 -15, 23, 31	
Errored	2^n-1, n = 5 - 15	
Marker density	1/8, 1/4, 1/2 ,3/4, 7/8 at 2^n-1, n = 5 - 15	
Extended one and zeros	2^n-1, n = 5 - 15	
	See Table 4 for further specifications	

4.2 16:1 Multiplexer E4868B

The MUX is a 3-slot VXI module. It is supplied with 16 x 2.7 Gbit/s or 3.35 Gbit/s differential data (DØ ... D15) from the tributary data generators. It can work with an internal clock (provided by the E4808A clock module) or with an external clock.

Three subrate clock outputs are available. They provide a 20 and 10 GHz clock signal and either a 2.7 GHz or a 675 MHz signal. High quality measurements require the 10 GHz/20 GHz clock outputs.

The data input multiplexes the data supplied at DØ ... D15 in a cyclical form.

The frequency relation of the parallel input ports and the serial output port need to be a 1:16 ratio with a fixed phase relation.

Table 2: MUX Module E4868B

Data Output	differential			
Format	NRZ			
Characteristics	50 Ohm, 1.85 mm Connectors			
Coupling	AC coupled			
Swing	500 mV ... 2V single ended, doubles differentially			
Swing Resolution	10 mV			
max. ext. Voltage	+/- 3 V			
On/Off	No relays provided, unused output needs external termination			
Transition Time (20/80)	9 ps typ.			
Jitter	< 1 ps rms, 700 fs rms typ.			
Offset control	±3 V			
Subrate Clock Outputs	3, single ended			
Rate (GHz)	½ and ¼ and 1/16 or 1/64 of data rate			
Output Characteristics	50 Ohm, 3.5 mm Connectors			
Coupling	AC coupled			
Output Swing and phase noise			**Level**	**Phase Noise @10 KHz offset**
	1/64	675 MHz	500 mVpp typ.	-100 dBc/Hz typ.
	1/16	2.7 GHz	300 mVpp typ.	not specified
	1/4	10.8 GHz	500 mVpp typ.	-81 dBc/Hz typ
	1/2	21.6 GHz	500 mVpp typ.	-75 dBc/Hz typ
External Clock Input	1, single ended			
Characteristics	50 Ohm, 3.5 mm Connector			
Coupling	AC coupled			
Frequency Range	9.5 to 10.8GHz or 19 to 21.6 GHz selectable			
Input Power	-10 dBm to 0 dBm			
Parallel Data Inputs	16, differential			
Format	NRZ			
Characteristics	50 Ohm, MCX Connectors			
Coupling	DC, center tapped to Ground			
Input Swing and Termination	400 mV around -200 mV (CML)			

Note: Recommended trigger source 10.8/21.6 GHz output.

4.3 1:16 Demultiplexer E4869B

Like the MUX module, this is a 3-slot VXI module. A 40G signal is demultiplexed in a cyclical way into 16 x 2.7 Gbit/s or 3.35 Gbit/s signals
(DØ ... D/15).

The data processing (individual BER analysis) is performed with the 16 tributary channels. The system software summarizes the measurements of each subrate channel and displays the result for the serial channel. The output timing of the DeMUX module data channels is automatically adjusted by the synchronization capability of the parallel analyzer channels.

The E4869B DeMUX module can operate in CDR (clock data recovery) mode or with an external clock. In CDR mode the alignment for the 50% criteria within the eye of the incoming signal is performed automatically. In external clock mode a delay adjustment between clock and data has to be performed externally. In both clock modes three subrate clock outputs are available that provide a 20 GHz/10 GHz clock
signal and a 2.7 GHz or 675 MHz clock signal.

To provide PRBS data at the serial side, PRWS (Pseudo-Random Word Sequence) data needs to be provided at the parallel side. 256 Mbits are available for memory-based patterns (16 channels x 16 MBits/channel).

The SONET/SDH editor automatically routes the cyclical data to the proper parallel channels.

Memory-based data can be used to generate a SONET frame. For OC-768 a SONET frame is 4,976,640 bits. The memory can store up to 25 frames.

Table 3: DeMUX Module E4869B

Modes	- Active CDR (Clock Data Recovery) / Phase Recovery (automatic sample point adjustment at 50% of the cycle) Ext. Clock Mode (sampling based on ext. clock)
Measurement	BER as summary of 16 parallel 2.7 Gbit/s or 3.35 Gbit/s channels
Data Input	differential
Characteristics	50 Ohm, 1.85 mm Connectors
Coupling	AC coupled
Sensitivity	50 mVpp typ.
Max Input amplitude	400 mVpp single ended
Absolute maximum input amplitude	600 mVpp
Maximum DC voltage	+/- 3 V
Format	NRZ
Threshold range	+/- 400 mV
Variable sampling delay	+/- 2 periods (ext clock) < 1 period (CDR mode)
Clock Data Recovery Bandwidth	> 1 MHz
Subrate Clock Outputs	3, single ended
Rate (GHz)	½ and ¼ and 1/16 of data rate
Characteristics	50 Ohm, 3.5 mm Connectors
Coupling	AC coupled
Swing	>400 mV (-4 dBm) fixed
External Clock Input	1, single ended
Characteristics	50 Ohm, 3.5 mm Connectors
Coupling	AC coupled
Frequency Range	9.5 to 10.8 GHz or 19 to 21.6 GHz selectable
Input Power	-10 dBm to 0 dBm
Parallel Data Outputs	16, differential
Format	NRZ
Characteristics	50 Ohm, MCX Connectors
Coupling	DC
Output Swing and Termination	400 mV around -200 mV (CML) into 2 x 50 Ohm center tapped to ground

Table 4a General Characteristics	Pattern Generator E4894B (43.2 Gbit/s)	Error Detector E4895B (43.2 Gbit/s)
Factory Installed	E8403A 13-slot VXI frame E8491B FireWire interface E4808A 10G clock module 8 x E4861A 2.7G module 16 x E4862B 2.7G generator front end E4868B 43.2GBit MUX module E4875A ParBERT software	E8403A 13-slot VXI frame E8491B FireWire interface E4808A 10G clock module 8 x E4861A 2.7G module 16 x E4863A 2.7G analyzer front end E4869B 43.2GBit DeMUX module E4875A ParBERT software
Operating Temperature Timing readjustment required if ambient temperature changes more than 2 deg, relative to the last calibration.	20° to 35°C	20° to 35°C
Storage	-20°C to + 60°C	-20°C to + 60°C
Power Requirements	90-264 Vac, ± 10%, 47-66 Hz	90-264 Vac, ± 10%, 47-66 Hz
Electromagnetic Compatibility	(EN55011/CISPR 11 group 1, class A + 26 dB)	(EN55011/CISPR 11 group 1, class A +26 dB)
Acoustic Noise	48 (56) dBA sound pressure at low (high) fan speed	48 (56) dBA sound pressure at low (high) fan speed
Safety	IEC 348, UL 1244, CSA 22.2#231, CE mark	IEC 348, UL 1244, CSA 22.2#231, CE mark
Physical Dimensions	W: 424.5 mm, H: 352 mm, D: 631mm,	W: 424.5 mm, H: 352 mm, D: 631mm,
Weight Net **Weight Shipping**	53 kg 105 kg	53 kg 105 kg

Table 4b General Characteristics	Pattern Generator E4896A (45 Gbit/s)	Error Detector E4897A (45 Gbit/s)
Factory Installed	E8403A 13-slot VXI frame E8491B FireWire interface E4808A 10G clock module 8 x E4861B 3.3G module 16 x E4862B 3.35G generator front end E4868B 45G MUX module E4875A ParBERT software	E8403A 13-slot VXI frame E8491B FireWire interface E4808A 10G clock module 8 x E4861B 3.3G module 16 x E4863B 3.3GB analyzer front end E4869B 45G DeMUX module E4875A ParBERT software
Operating Temperature Timing readjustment required if ambient temperature changes more than 2 deg, relative to the last calibration.	20° to 35°C	20° to 35°C
Storage	-20°C to + 60°C	-20°C to + 60°C
Power Requirements **Electromagnetic Compatibility**	90-264 Vac, ± 10%, 47-66 Hz (EN55011/CISPR 11 group 1,	90-264 Vac, ± 10%, 47-66 Hz (EN55011/CISPR 11 group 1,
Acoustic Noise	class A + 26 dB) 48 (56) dBA sound pressure at low (high) fan speed	class A +26 dB) 48 (56) dBA sound pressure at low (high) fan speed
Safety	IEC 348, UL 1244, CSA 22.2#231, CE mark	IEC 348, UL 1244, CSA 22.2#231, CE mark
Physical Dimensions	W: 424.5 mm, H: 352 mm, D: 631mm,	W: 424.5 mm, H: 352 mm, D: 631mm,
Weight Net **Weight Shipping**	53 kg 105 kg	53 kg 105 kg

Table 5: Power Requirements of Modules and Front-Ends							
Modules	**dc Volts**	**+24 V**	**+12 V**	**+5 V**	**-2 V**	**-5.2 V**	**-12 V**
E4808A High	dc Current	.35 A	.2 A	3.0 A	1.2 A	3.6 A	0.2 A
Performance Clock Module	Dynamic Current	0.04 A	0.02 A	0.3 A	0.12 A	0.36 A	0.02 A
E4861A 2.7 Gbit/s Module	dc Current	0.10	0.50 A	5.20 A	1.80 A	4.00 A	0.90 A
	Dynamic Current	0.01 A	0.05 A	0.52 A	0.18 A	0.40 A	0.09 A
E4861B 3.35 Gbit/s Module	dc Current	0.02 A	0.02 A	1.8 A	0.33 A	0.04 A	0 A
	Dynamic Current	0.01 A	0.01 A	0.2 A	0.03 A	0.05 A	0 A
E4868B 45 Gbit/s MUX Module	dc Current	0.3 A	0.9 A	2.8 A	0.15 A	1.2 A	0.9 A
	Dynamic Current	0.04 A	0.3 A	0.4 A	0.01 A	0.2 A	0.2 A
E4869B 45 Gbit/s DeMUX Module	dc Current	0.3 A	0.9 A	3.5 A	0.1 A	0.7 A	0.7 A
	Dynamic Current	1.06 A	0.2 A	0.6 A	0.01 A	0.2 A	0.2 A

* These specifications are valid for the module with the front ends installed

Table 6: Cooling requirements for the modules E4808A and E4861A with the front-ends installed		
Modules	ΔPP mm H_2O for	Air Flow
	10°C rise	Liter/s
E4808A	0.25	3.6
E4861A	0.4	5.2
E4868B	tbd	tbd
E4869B	tbd	tbd

These specifications describe the instrument's warranted performance to 43.2 Gbit/s (E4894B, E4895B) or to 45 Gbit/s (E4896A, E4897A). Non-warranted values are described as typical. All specifications are valid from 20°C to 35°C at constant ambient temperature after a thirty minute warm-up phase, with outputs and inputs terminated with 50 Ω.

5.0 Optical Interface and the Specifications of the Electrical/Optical System

The optical interface expands the Agilent ParBERT 81250 40G BER test system to the full electrical/optical capability. ParBERT 40G Electrical/Optical is a fully integrated, scalable bit error ratio test system that generates and analyzes optical or electrical data streams up to 45 Gbit/s (subject to the configuration).

Figure 22: Agilent E4883A and E4882A Optical/Electrical Modules

45G Optical-Electrical Modules

The new ParBERT 45G E/O and O/E modules work in conjunction with the electrical ParBERT modules. Upgrades are available.

The **E4882 45Gbit/s Lightwave Recaiver** is a 1-slot amplified O/E converter that connects to the optical output of the DUT and to the input of the ParBERT 38 - 45G electrical DeMUX module.

The **E4883A Lightwave Transmitter** is a 2-slot module that connects to the ParBERT 38 - 45G electrical MUX module and the DUT optical input.

The Lightwave Transmitter module can output NRZ, RZ and RZ-CS data formats.

The **E4884A High Performance option** provides enhanced wavelength tunability and variable output power using external equipment to cover the C- and L-band.

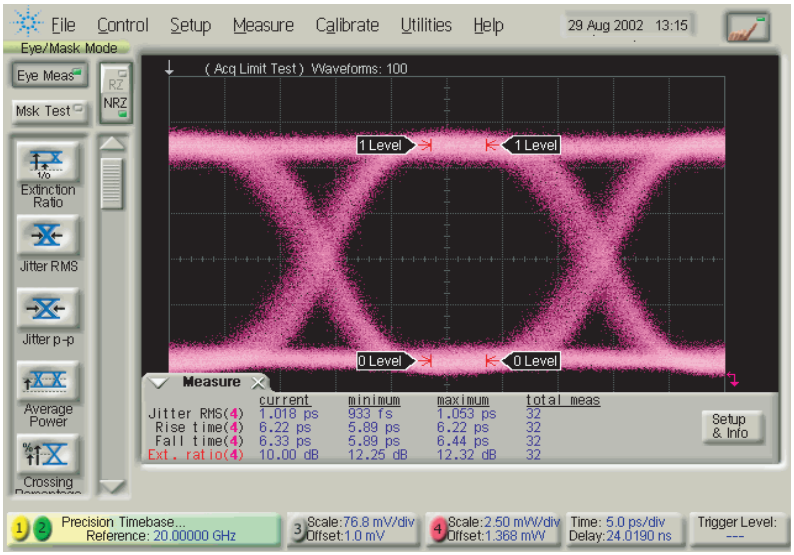


Figure 23: E4883A Lightwave Transmitter output viewed on Agilent 86116B (65 GHz Optical Module)

5.1 ParBERT 81250 45G Electrical/Optical BER Test System - Technical Specifications

	E4883A 45 Gbit/s Lightwave Transmitter with internal 1550 nm DFB Laser	**E4884A** 45 Gbit/s High Performance Lightwave Option for E4883A	**E4882A** 45 Gbit/s Lightwave Receiver
Description	2-slot VXI module	Additional Test Instruments Option 001 High Performance C and L Band Transmitter	1-slot VXI module
Input/Output	**Electrical Inputs:** Data Input: 1.85 mm RZ Clock Input: 3.5 mm **Optical Inputs:** Laser Input: FC/PC; PMF; 40mW maximum **Optical Outputs:** Data Output: FC/APC; adapters available for other connector types **Internal Laser Output:** FC/PC; PMF; 40 mW	**<u>High Performance Transmitter</u>** Includes: - C and L Band Optical Amplifier - 8164B Lightwave Measurement System - 81635A Dual Power Sensor Module - 81567A Optical Attenuator with Power Control Module - 81642B High Power Tunable Laser Module - Software for High Performance Transmitter Enhancement - Required optical interconnect cables	**Electrical Outputs:** Data Output: 1.85 mm **Optical Inputs:** Data Input: FC/APC; adapters available for other connector types
Key Specifications	**Specifications apply when used with E4868B** **Data Rate:** 38 - 43.2 Gbit/s; over programming to 45 Gbit/s **Jitter:** To Be Defined **Wavelength:** 1550.12 nm internal laser; 1530 - 1605 nm using external laser source **Modulation:** Mach-Zehnder modulator NRZ, RZ, RZ-CS **Output Power:** > 0 dBm **Extinction Ratio:** > 10 dB **Rise time:** < 10ps **Fall time:** < 10ps	**<u>High Performance Transmitter</u>** **Specifications apply when used with E4868B and E4883A** **Specifications of E4883A apply except as noted.** **Wavelength:** 1530 nm - 1565 nm and 1570 - 1605 nm **Output Power:** +5 dBm to -40 dBm **Extinction Ratio:** 9 dB (typical)	**Specifications apply when used with E4869B** **Data Rate:** 38 - 43.2 Gbit/s; over programming to 45 Gbit/s **Jitter:** To Be Defined **Wavelength:** 1520 - 1640 nm **Modulation:** NRZ, RZ, RZ-CS **Input Sensitivity:** -5 dBm at 1550 nm with PRBS 2^{23}-1 at BER 10^{-10} at OC-768 **Conversion Gain:** > 50 V/W **Maximum Optical Input Power:** +4 dBm
Operating Characteristics	**Data Rate Range:** NRZ 2.5 - 43.2 Gbit/s; RZ 38 - 43.2 Gbit/s **Insertion Loss of external Laser Input:** < 16 dB nominal **External Wavelength Range:** 1520 - 1640 nm **Wavelength Stability:** + - 3ppm - 15 minutes **Output Power Stability:** To Be Defined **Rise time:** < 8ps typical **Fall time:** < 8ps typical **Jitter:** < 1.2 ps rms (typical) **RZ Duty Cycle Adjustment:** 30% - 45% (typical) **Chirp:** +- 0.5 alpha		**Data Rate Range:** 2.5 - 43.2 Gbit/s **Input Sensitivity:** -9 dBm at 1550 nm of E4882A alone; < -15dBm sensitivity available with reduced wavelength range - contact factory **Input Damage Threshold:** +10 dBm **Maximum Optical Input for Linear Operation:** +7 dBm **Jitter:** < 1.5 ps rms (typical)

6.0 ParBERT 40G Product Structure

Warranty & Services

- All modules have 3 years Return to Agilent warranty (if bought as separate pieces).
- All bundles (81250A, E4894A/95A/94B/95B/96A/97A) have 1 year on-site warranty.
- An on-site repair contract or Return to Agilent contract can be purchased once the 1 year on-site warranty has expired.
- Additional on-site warranty can be chosen for 3 or 5 years.
- On-site productivity assistance is included in the bundles.
- Standard compliant and commercial calibration can be chosen for 3 or 5 years.
- Commercial calibration is NOT automatically included.

Product	Option	Description	Products Included
E4894B		43.2 Gbit/s Pattern Generator	Includes on-site productivity assistance, 1 x E8403A, 1 x E4808A, 1 x E8491B + E8491B Opt. 001, 8 x E4861A, 16 x E4862A, 1 x E4868B, 1 x 15446A, 1x E4875A
	001	10.8G Analyzer Add-On	Includes E8403A, E4808A, 4 x E4867A, E8491B
	002	10.8G Generator & Analyzer Add-On	Includes E8403A, E4808A, 4 x E4867A, 4 x E4866A, E8491B
E4895B		43.2 Gbit/s Error Detector	Includes on-site productivity assistance, 1 x E8403A, 1 x E4808A, 1 x E8491B + E8491B Opt. 001, 8 x E4861A, 16 x E4863A, 1x E4869B, 1x E4875A
	001	10.8G Generator Add-On	Includes E8403A, E4808A, 4 x E4866A, E8491B
E4896A		45 Gbit/s Pattern Generator	Includes on-site productivity assistance, 1 x E8403A, 1 x E4808A, 1 x E8491B + E8491B Opt. 001, 8 x E4861B, 16 x E4862B, 1 x E4868B, 1x E4875A
	001	10.8G Analyzer Add-On	Includes E8403A, E4808A, 4 x E4867A, E8491B
	002	10.8G Generator & Analyzer Add-On	Includes E8403A, E4808A, 4 x E4867A, 4 x E4866A, E8491B
	003	Add one extra 3.35G Generator	Includes E4861B, E4862B
	004	Add two extra 3.35G Generators	Includes E4861B, 2 x E4862B
	005	Add one extra 3.35G Analyzer	Includes E4861B, E4863B
	006	Add two extra 3.35G Analyzers	Includes E4861B, 2 x E4863B
E4897A		45 Gbit/s Error Detector	Includes on-site productivity assistance, 1 x E8403A, 1 x E4808A, 1x E8491B + E8491B Opt. 001, 8 x E4861B, 16 x E4863B, 1 x E4869B, 1x E4875A
	001	10.8G Generator Add-On	Includes E8403A, E4808A, 4 x E4866A, E8491B
E4883A		45 Gbit/s Lightwave Transmitter with internal 1550nm DFB Laser	
E4884A		45 Gbit/s High performance Lightwave option	C+L Band optical ampl., 8164A, 81635A, 81567A, 81642B, Software
E4882A		45 Gbit/s Lightwave Receiver	
E4860AS	014	External PC	256MB, 6Gb HDD Pentium IV - without PC-accessories 15444A
	020	Rack	1 x 3662B
	432	Upgrade from E4868A to E4868B	
	433	Upgrade from E4869A to E4869B	
	540	External amp for 40G generator	
	270	Upgrade for one module from 2.67 Gbit/s to 2.7 Gbit/s	
E4832A		675 MHz Gen./An. Module	
E4838A		Differential Generator Front-End, 675 MHz	
E4835A		Two Differential Analyzer Front-Ends, 675 Msa	
E4875A		One licence and software CD ROM for ParBERT 81250	

Accessories

Cable accessories up to 3.35 Gbit/s	
15440A	Adapter kit: 4 x SMA (M) I/O adapters
15442A	Cable kit: 4 x SMA (m) to SMA (m)
15443A	Matched cable pair
Computer accessories	
15444A	Keybord, mouse, 17"monitor
15445A	External CD-ROM
Clock Module accessories	
15446A	8-line trigger input pod
15447A	Deskew Probe 1144A
Test Fixture accessories	
E4839A	Test fixture
15441A	Cable kit: 10 x SMA (m) to SCI connector
15448A	Pogo cable kit: 4 x SMA(m) & 2 Pogo adapter
15449A	DUT board 50 Ohm impedance
10 Gbit/s Module accessories	
N4869A	Cable Kit: 3 cables with phase adjuster for connecting E4866A with N4868A
N4870A	Cable Kit: 2.4mm for N4868A output
N4871A	Cable Kit: SMA matched pair, 50ps

On-site Installation

Delivery of the system is followed by an on-site visit from experienced Agilent personnel to ensure the system has arrived meeting its performance requirements.

Productivity Assistance

Productivity assistance is provided with ParBERT 40G and is designed to introduce users to the system components, the graphical user interface (GUI) and the programming interface. Productivity Assistance is delivered on-site and will include the following topics:

- Overview of system functions and capabilities
- General steps for setting up measurements
- Review of system documentation, diagnostics and architecture.

For details, please refer to the Data Sheet 5980-2160EN.

Related Literature	Pub. Number
Brochure "Need to Test BER?"	5968-9250E
Agilent ParBERT 81250, MUX/DeMUX Application, Application Note	5968-9695E
Agilent ParBERT 81250 Parallel Bit Error Ratio Tester, Photo Card	5980-0830E
Agilent Productivity Assistance	5980-2160EN
Agilent ParBERT 81250 Parallel Bit Error Ratio Tester Product Overview	5968-9188E
Need to Test 40 Gb/s? Brochure	5988-2038EN
ParBERT 81250 Technology Refresh	5988-4174ENUC
Agilent E2150B 43G E/O BER System	5988-5892EN
Measuring a 40G eye Pattern	5988 6625EN
ParBERT 81250 Automatic Phase Margin Measurements at 40G	5988-5654EN

For more information, please visit us at:
www.agilent.com/comms/40G
www.agilent.com/find/parbert

Agilent Email Updates

www.agilent.com/find/emailupdates

Get Free Email Updates

Keep up to date with Agilent's free Email Updates. As a subscriber, you will receive regular, customized email updates on the topics you select. Updates cover support, products and services, applications, promotions, events, and other areas. It is easy to unsubscribe or change your preferences. Subscribe today: http://www.agilent.com/find/emailupdates.

Agilent is committed to respecting and protecting your privacy. Our Privacy Statement at http://www.agilent.com/go/privacy describes our commitment to you. Please direct any questions about Agilent's privacy program to privacy_advocate@agilent.com.

Agilent Technologies' Test and Measurement Support, Services, and Assistance

Agilent Technologies aims to maximize the value you receive, while minimizing your risk and problems. We strive to ensure that you get the test and measurement capabilities you paid for and obtain the support you need. Our extensive support resources and services can help you choose the right Agilent products for your applications and apply them successfully. Every instrument and system we sell has a global warranty. Support is available for at least five years beyond the production life of the product. Two concepts underlie Agilent's overall support policy: "Our Promise" and "Your Advantage."

Our Promise

"Our Promise" means your Agilent test and measurement equipment will meet its advertised performance and functionality. When you are choosing new equipment, we will help you with product information, including realistic performance specifications and practical recommendations from experienced test engineers. When you use Agilent equipment, we can verify that it works properly, help with product operation, and provide basic measurement assistance for the use of specified capabilities, at no extra cost upon request. Many self-help tools are available.

Your Advantage

"Your Advantage" means that Agilent offers a wide range of additional expert test and measurement services, which you can purchase according to your unique technical and business needs. Solve problems efficiently and gain a competitive edge by contracting us for calibration, extra- cost upgrades, out-of-warranty repairs, and on-site education and training, as well as design, system integration, project management, and other professional services. Experienced Agilent engineers and technicians worldwide can help you maximize your productivity, optimize the return on investment of your Agilent instruments and systems, and obtain dependable measurement accuracy for the life of those products.

Get assistance with all your test and measurement needs at:
www.agilent.com/find/assist

Or check your local phone book for the Agilent office near you.

Printed in the Netherlands March 13th, 2003
5988-3020EN

Agilent Technologies